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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,073	02/25/2004	Teruo Takizawa	118439	8936

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EXAMINER	
QUINTO, KEVIN V	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/785,073	TAKIZAWA, TERUO	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2 and 6-8* is/are allowed.

6)☒ Claim(s) *1 and 3-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *25 February 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi (United States Patent Application No. US 2003/0197598 A1) in view of Brown et al. (USPN 6,417,526 B2) and further in view of Streetman ("Solid State Electronic Devices," p. 205).

4. With regard to claim 1, Hayashi (United States Patent Application No. US 2003/0197598 A1) discloses a similar device. Figures 9 and 10 of Hayashi disclose a semiconductor device with a bridge rectifier circuit (3 in figure 9, figure 10 has added detail) having a plurality of diodes (D1-D4, figure 10). Hayashi does not disclose the use of diode which uses a p-type silicon layer containing germanium and an n-type silicon layer junctioned to the p-type silicon layer. However the use of such diodes is well known in the art. Brown et al. (USPN

6,417,526 B2, hereinafter referred to as the "Brown" reference) discloses a diode (in figure 1) that has a p-type silicon layer (1) containing germanium and an n-type silicon layer (2) junctioned to the p-type silicon layer (1). Brown states that such a diode has a short switching time (column 6, lines 33-40). Streetman ("Solid State Electronic Devices," p. 205) states that diodes with a fast switching speed are desirable in the art. In view of Streetman, it would therefore be obvious to implement the Brown diode in the bridge rectifier circuit of Hayashi.

5. In reference to claim 4, the bridge rectifier circuit (3, figure 9) of Hayashi has a plurality of diodes (D1-D4, figure 10) which rectify a predetermined alternating-current voltage to a direct-current voltage.

6. With regard to claim 5, figure 9 of Hayashi shows that the semiconductor device has a coil antenna (L1) coupled to one side of the bridge rectifier circuit (3); a smoothing capacitor (Ca) coupled to the other side of the bridge rectifier circuit (3). The coil antenna (L1) generates an alternating-current voltage by electromagnetic induction. The bridge rectifier circuit (3) rectifies the alternating-current voltage into a direct-current voltage. The smoothing capacitor (Ca) smoothes the direct-current voltage into a constant voltage.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi (United States Patent Application No. US 2003/0197598 A1) in view of Brown et al. (USPN 6,417,526 B2) and further in view of Streetman ("Solid State Electronic Devices," p. 205) as applied to claim 1 above and further in view of Kanbara et al. (USPN 4,575,925).

8. In reference to claim 3, neither Hayashi nor Brown discloses the use of an insulating substrate with the diode. However the use of such substrates is well known in the art. Kanbara et al. (USPN 4,575,925, hereinafter referred to as the "Kanbara" reference) discloses that the use of an SOI substrate (an insulating substrate) leads to a device with the benefits of a low stray capacity and a high breakdown voltage (column 1, lines 19-27). In view of Kanbara, it would therefore be obvious to implement the diode of Brown on an insulating substrate.

Allowable Subject Matter

9. Claims 2 and 6-8 are allowed.

10. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests a fabrication process for a semiconductor device which contains a diode that has a p-type silicon-germanium mixed crystal layer (attained by ion implanting germanium into silicon) and an n-type silicon layer junctioned to the p-type silicon-germanium mixed crystal layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The

fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

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